HARDWARE-EFFICIENT IMPLEMENTATION OF DYNAMIC ELEMENT MATCHING IN SIGMA-DELTA DAC'S

updated

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application No. 10/354,159, filed January 30, 2002, which claims priority to U.S. Provisional Application No. 60/350,386, filed January 24, 2002, entitled Dynamic Element Matching Technique for Linearization of Unit-Element Digital-To-Analog Converters, and is related to U.S. Patent Application No. 10/225,353, filed August 22, 2002, entitled Shuffler Apparatus and Related Dynamic Element Matching Technique for Linearization of Unit-Element Digital-To-Analog Converters, all of which are incorporated herein by reference in their entirety.

is now a U.S. Patent 6,795,003

BACKGROUND OF THE INVENTION

[0002] In high resolution digital-to-analog converters (DACs), performance metrics such as linearity and noise are nominally determined by the matching of parameters derived from physical quantities in the construction of the DACs on an integrated circuit (IC), such as width, length, thickness, doping, etc. As a general rule, for each additional bit of performance in the DAC, parameter matching needs to be twice as tight. This translates to an increase by a factor of four in the IC area required by the DAC. When the DAC resolution is in the 16-bit range, it is no longer practical/economical to use size alone to achieve the required matching.

[0003] Over-sampled (sigma-delta) DACs (also referred to as "converters") alleviate the need for raw matching using single-bit conversion (so called 1-bit DACs in CD players). A single-bit DAC has only two points in a transfer function of the DAC, and thus is inherently linear. The function of a sigma-